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POLYMER MODULATOR CONTACT POLING GUIDE

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APPROVED: /s/

ANDREW R. PIRICH
Chief, Photonics Technology Branch
Rome Operations Office
Sensors Directorate

FOR THE DIRECTOR: /s/

RICHARD G. SHAUGHNESSY, Lt Col, USAF
Chief, Rome Operations Office
Sensors Directorate

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AFRL Project Engineer: Brian M. Flusche, 1Lt., USAF/SNDP/ (315) 330-4269/ Brian.Flusche@rl.af.mil

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13. ABSTRACT ***(Maximum 200 Words)***

This guide documents the polymer modulator contact poling procedures developed by AFRL/SNDP between 5 Aug 02 and 5 Aug 04, as well as observations and lessons learned during that time. A partly automated, highly functional poling setup is described. CPW-1 material samples were tested to determine the optimum poling protocol. Modulators fabricated with a core material consisting of 25% CPW-1 by weight in amorphous polycarbonate (APC) yielded a 4.6 volt $V\pi$. The feasibility of poling an entire wafer at a time was examined, and challenges identified. Another set of modulators were fabricated using deuterated methanol and a core consisting of 29% CPW-1 in APC. The best of these devices yielded a 4.2 volt $V\pi$ fand losses comparable to the 25% CPW-1 devices, indicating that deuterated methanol possibly reduces loss. 550 volts was determined to be the optimum poling voltage. Another set of devices were fabricated with a core of 35% FN3, a chromophore developed in-house. The best of these devices yielded a 20 volt $V\pi$ Among key poling issues examined were the appropriate poling temperature, the appropriate time to apply voltage to a sample, and the optimum amount of voltage to apply during poling. Poling induced bleaching is observed. A discussion is included on the information that can be gained from measuring current during poling and observing the profile produced.

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1 Background

1.1 Mission

An essential part of the mission of the AFRL/SNDP RF Links team is to optimize the electro-optic (EO) effect of nonlinear optical chromophores for polymer modulators to be used in high speed, high bandwidth fiber optic links. All modulators and bulk material samples fabricated during this time were poled through contact poling, as opposed to corona poling. The end effect on the chromophore molecules is the same, but each method presents some unique challenges.

1.2 Measures of Merit

Two measures of merit for these modulators are Vπ and optical loss. Vπ is the amount of voltage needed to induce a 180° phase shift between input and output light of one arm of a modulator inducing a full swing from maximum light output to minimum light output. Vπ is dependent on the electro-optic coefficient (r33) of a given chromophore, with a high r33 contributing to a low Vπ. Major contributors to optical loss are the amount of light absorbed by the chromophore molecules and the amount of light scattered out of the waveguide in question. Absorption and r33 are material properties that can be controlled by chromophore loading density[1].

1.3 Modulator Explanation

1.3.1 Device Construction

Our modulators are three layer polymer stacks spun onto a metalized silicon wafer, with a gold electrode patterned on top. The metalized silicon wafer serves as a ground plane electrode. The lowest layer of the polymer stack is a lower cladding, the middle layer is a core material filled with electro-optically active chromophore molecules, and the upper polymer layer is an upper cladding. As shown in Figure 1-1. Polymer Modulator, we define a Mach Zhender modulator (MZM) in the optically guiding center or core layer. In this design a laser beam is coupled into the modulator, is split evenly into two legs, and recombined upon leaving the modulator.

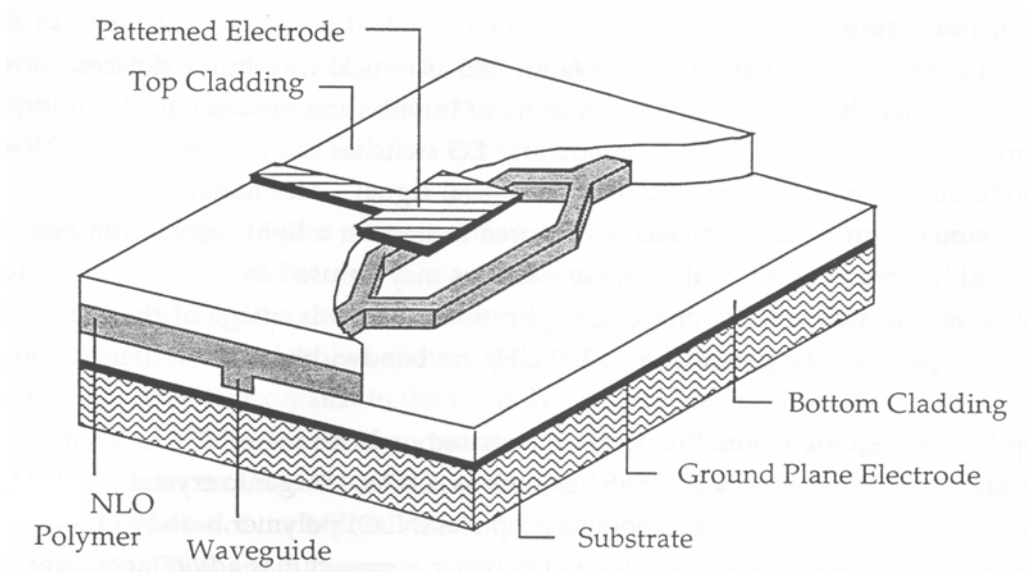

Figure 1-1. Polymer Modulator

1.3.2 Electro-Optic Effect

We modulate the laser beam by applying a voltage to one of the arms, and changing the index of refraction in this arm. The change in index of refraction in turn changes the optical path length in one arm. This means that when the light recombines, the intensity changes because of constructive and destructive interference. The index change is caused by the EO effect of the molecules in the core. These molecules are essentially dipoles, which must all be oriented in the same direction in order to maximize their EO effect. This orientation occurs through a process called poling.

1.4 Poling

1.4.1 Initial conditions

When the modulator or material sample is first completed, it is a solid at room temperature. The chromophore molecules are randomly aligned and fixed in place.

1.4.2 General Process

The MZM is heated over some time period to the glass transition temperature (Tg) of the material. The Tg is based on the loading density of chromophore molecules and the type of host material. Once the core material reaches the Tg, the material becomes “gooey” and the mobility of the guest chromophore in the polymer host is increased. At temperature, a strong electric field is then applied to line up the dipole chromophore molecules. The sample is then cooled while still under voltage. This process aligns the chromophores and locks them in position, producing a material with ideally a high r33 and a device with a low $V\pi$.

1.4.3 Challenges

Water, light and oxygen can degrade the EO effect of the chromophore molecules. First, chemical reactions can occur resulting in chromophore bleaching, where the material becomes very optically lossy. Second, excess energy in the poling process can rip molecules apart, reducing the overall EO effect because there are now fewer active chromophore molecules.

2 Setup Description

2.1 *Interim Poling Setup*

This poling setup was conceived as a quick way to provide us an initial capability. After working on this setup, we took lessons learned forward to planning for a more ideal setup.

2.1.1 Poling Box Structure

The interim poling setup, used primarily to support our Teng & Man testing described in Section 5, consisted of a Plexiglas box that was taped down to an optical table on all four sides. The top of the box was mounted with hinges to the back of the box, allowing the top to swing open to insert and remove samples. A hole had been drilled in the back of the box, allowing us to place a hot plate in the box and run the wiring out the rear of the box to the Sigma temperature control unit. Another hole was for flexible plastic tubing that led back to a compressed nitrogen cylinder. Gaps around these holes were taped over with our flexible tack tape. A hole was also drilled in the left and right sides of the box to allow our probe arms into the box. The holes were covered with scraps of purple nitrile gloves taped to the box with blue tape. The hope was that the nitrile would provide a flexible seal between the box and the probe arms.

2.1.2 Electrical Probe Connections and Concerns

On top of the hot plate was a sapphire wafer, which electrically insulated the sample under test from the metal hot plate. The sapphire wafer was held in place by a metal clip attached to the hot plate. The probe tips used were standard Alessi pointed tips, which we would bend to form a “U” shape. We used the bottom of the “U” shape to touch down onto the electrode. We used an Oriel high voltage source, with an ammeter and our hot probe hooked in series. The ammeter was a digital Fluke meter, capable of reading only tenths of microamps of current. The hot probe would touch down on the top gold electrode of our sample, and the circuit would be completed by touching a probe down to ground electrode.

2.1.3 Placing the Probe

A microscope was placed on the optical table near the box and was mounted so that the user could swing it into position and look down on the sample to assist with probe placement. A fiber optic illuminator provided the needed light for the microscope, and allowed the user to keep the room lights off.

2.2 Principal Poling Setup

2.2.1 Poling Box Structure

We bought a stainless steel glove box from Terra Universal to build this setup. A picture of the setup is shown in Figure 2-1. Stainless Steel Glove Box. The glove box has a vacuum oven airlock on one side and a plain airlock on the other. The box is also equipped with an oxygen sensor that reads percent oxygen down to tenths of a percent. Another key capability is a humidity sensor combined with a regulator. This sensor allows the user to set a constant flow of nitrogen into the box, and also activates a 30 psi burst of nitrogen when the humidity level exceeds the threshold set by the user. We made a cover for the front window on the box out of black cloth that could be secured in place with Velcro, keeping all light out of the box. Our temperature controller and hot plate was a Sigma unit.

Figure 2-1. Stainless Steel Glove Box

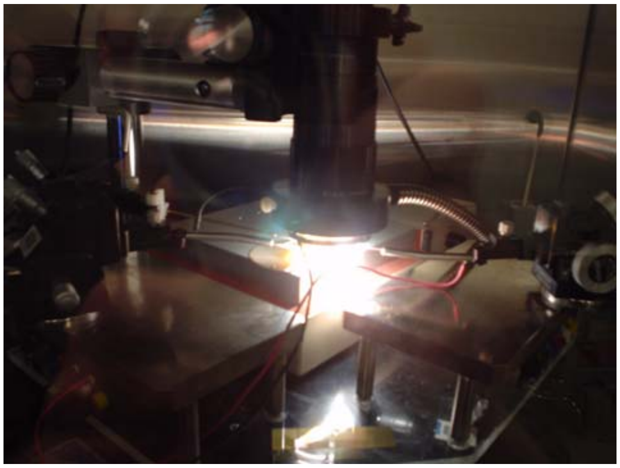

Figure 2-2. Probe Setup Inside Glove Box

2.2.2 Electrical Probe Connections and Concerns

A key component of this setup was a Keithley 2002 digital multimeter capable of reading 8 ½ digits. This is essential to accurately tracking current data during device level poling. The sample was placed on top of a sapphire wafer on the hot plate. In order to help place the probes, a camera was attached to a microscope objective, with a ring light source attached to the bottom of the microscope objective. The camera output was wired out the back of the glove box to a television monitor on the outside. We had to use carbide drill bits to drill through the stainless steel back of the box in order to run these cables. We then sealed around the cables with duct seal. The power supply was an SRS unit capable of sourcing up to 5,000V. The hot plate, ammeter, and power supply were all controllable through a GPIB interface. Inside the glove box is a probe station that fits around the hot plate. The probe station and hot plate were mounted on a stage that could be moved along two axes for ease of viewing through the camera.

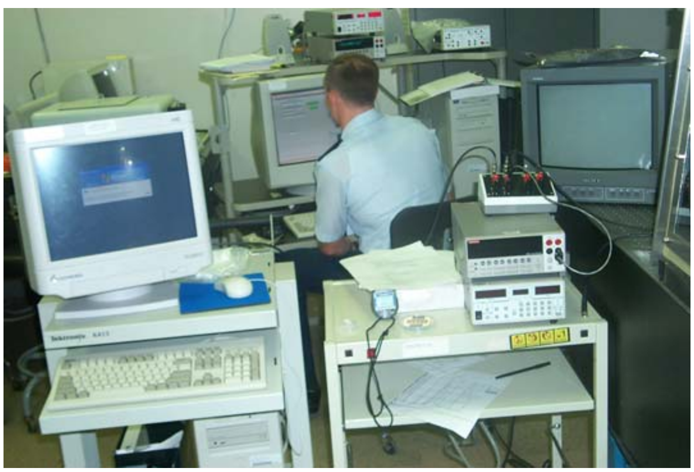

Figure 2-3. Measurement Instrumentation Used in Setup

2.2.3 Probe Tip

We made a tip out of wire cut off of a resistor and soldered to a relatively flat, relatively flexible copper piece from a rotary switch. We named this our shovel probe, since the profile it created upon touching down on the sample resembled the wide curved back of a shovel. This probe was superior to both the standard Alessi probe tip and a cat whisker probe.

3 Troubleshooting Quick Reference

3.1 Chip Preparation

3.1.1 Chip is shorted when tested before poling run

If probes are placed before any heating is applied and a chip is found to have a short, the likely cause is some gold lapping over the edge of the chip, connecting the upper electrodes to the lower ones. The solution is to polish the edges of the chip by hand on the disc shaped polishing paper in the clean room.

3.1.2 Vacuum oven will not function correctly

Check to make sure the vacuum pump is on, the oven valve to vacuum pump is open, the oven valve to nitrogen cylinder is closed, and the nitrogen cylinder is off. If the oven still will not evacuate, the solution is to press inward on the glass at the oven/room interface while lifting the edge of the oven underneath the door.

3.2 Poling Chamber Preparation

3.2.1 Oxygen sensor not reading percent oxygen

The Oxygen sensor takes 30 minutes to warm up. Until that time, the display reads the temperature of the sensor, which must be 750° C to function.

3.2.2 Setup uses nitrogen too fast

Ensure that the regulator on the nitrogen tank is set to approximately 23. Ensure humidity sensor is set to 6.0 percent humidity. Ensure the flow meter on the humidity sensor is set to max during chamber purge, and 17 thereafter. Ensure purge strength, the dial on the right, is set to 20-30.

3.3 Performing a poling run

3.3.1 Measurement equipment not talking with computer

Ensure that LabVIEW has been exited and restarted before poling if used in an earlier run. Ensure that all measurement equipment was turned on after the LabVIEW program was opened. The way the program is written, if the measurement equipment is turned on before LabVIEW is opened the program will not recognize the equipment is present.

3.3.2 "I trip" error message encountered on power supply

The chip has shorted out, possibly because the "hot" probe is being applied with too much pressure. When dropping the probe, pay special attention to apply pressure only until the probe begins to slide forward.

3.3.3 "V trip" error message encountered on power supply

This means the load on the power supply is changing too rapidly. A couple of different things could cause this. First, ensure the supply's voltage limit is set far above (perhaps 4x) the amount of peak voltage you intend to use. Second, determine whether the voltage trips are causing damage where the probe contacts the chip or at some other place on the chip. If damage is apparent directly under the probe, there is too much current flowing through too thin a gold pad. A possible solution is to reposition the probe on a thicker area of gold that can support this. If the area under the probe is intact, then it is likely that material defects are to blame. If possible, in future fabrication runs, ensure there is no shorting of the top metal to the silicon wafer at the edge. Otherwise, cleave extra parts of wafer off the edges to eliminate this area.

3.3.4 Graph of current value full of spikes

If the current value is changing between near zero and some higher value, this indicates the probe is bouncing as the chip is heating up and expanding. To fix the problem, reposition the probe and ensure to apply with enough pressure, keeping in mind that when the material is hot it is very soft.

4 Poling Quick Reference Checklist

This information documents the process to get a 4.2V Vπ on 2cm chips from the Dec 03 fabrication run. Chips made of 29% CPW1 with deuterated methanol.

Chip Preparation

1) Select chips for poling and scrape a ground electrode on each.
2) Put chips in oven on aluminum boat and close oven
3) Open vacuum line, turn on vacuum pump
4) Push up on end of oven and in glass part of oven door until vacuum gauge indicates suction
5) Allow oven to pump down to 50 kPa on gauge
6) Turn on nitrogen cylinder connected to oven
7) Open nitrogen line, allow nitrogen to flow until gauge reads 10 kPa, close nitrogen line
8) Repeat step 7 twice with vacuum applied to flush out the chamber
9) Turn off nitrogen cylinder connected to oven
10) Let chips bake out a minimum of 3 hours

Poling Chamber Preparation

1) Turn on oxygen sensor by using green button on the front

   Note: Will not read percent oxygen until its had 30 minutes to warm up
2) Open nitrogen cylinder on line attached to poling box
3) Turn on humidity sensor by using black switch in back
4) Using black dial on left of humidity sensor, set flow to more than 20

Performing A Poling Run

1) Do not begin until oxygen sensor reads percent oxygen below 2.0
2) Check nitrogen tank hooked to poling box; if below 1000 psi, change before executing poling run
3) Using black dial on left of humidity sensor, set flow to 17
4) Turn on nitrogen cylinder hooked to vacuum oven
5) Turn off vacuum pump, on oven close vacuum line then open nitrogen line
6) After bringing the oven to equilibrium pressure, the sound of nitrogen flow will change
7) Close nitrogen line on oven, turn off nitrogen cylinder hooked to vacuum oven
8) Remove desired chip from oven, place on sapphire wafer
9) Put remaining chips back in oven, close oven, and open vacuum line
10) Turn on vacuum pump
11) Begin vacuuming out oven by pushing up on end of oven and pushing in on glass in oven door
12) Turn on TV monitor, camera, and light source for microscope
13) Place ground probe
14) Turn off TV monitor, camera, and light source, close Velcro curtain
15) Open LabVIEW device poling program
16) Turn on power supply and multimeter, set temperature controller dial to remote mode

17) In LabVIEW, insert name of chip before temp, voltage, and current in each file name above the graphs to save data to the RF Links team shared folder under poling data

18) Set the voltage step timer to 250 ms

19) Set first ramp time to 15 minutes

20) Set plateau time to 10 minutes

21) Set plateau temperature to 120 degrees

22) Set second ramp time to 15 minutes

23) Set poling time to 28 minutes

24) Set poling temperature to 150 degrees

25) Begin LabVIEW program by clicking arrow at top left – start handheld stop watch at same time

    a. LabVIEW programs are stored in the LabVIEW directory on the computer in Lab 10

    b. Select either WaferPoling.vi or DevicePoling.vi as appropriate

26) Check to ensure power supply, multimeter, and temperature controller are in remote mode and functioning (reading/reporting data and heating)

27) Turn off room lights – you're free until 48 minutes on the stop watch; use this time for making lab book entries, etc

28) At 48 minutes on the stop watch, begin the process of setting the hot probe down

    a. Turn on TV monitor, camera, and light source

    b. Open Velcro curtain and place hot probe on electrode

c. Turn off TV monitor, camera, light source, and close curtain

d. Type 100 volts in voltage block on LabVIEW program

e. Hit update voltage button, observe current profile

f. If a steady, linear current increase is observed, quickly type 550 volts in voltage block and hit update voltage when power supply reaches 100 volts

g. If current remains bouncing around a flat line, you have missed the probe placement. Return voltage to zero and repeat the process from step “a”

29) Observe current profile on LabVIEW to ensure probe stays down; poor probe placement is marked by current “bouncing” between some value and zero

30) Cooling will begin at 1 hour 8 minutes on the stopwatch

31) You can leave, but check on voltage & current every 10 minutes - Allow the sample to cool to 40 degrees C or below

a. Should take about 2.5 hours from 150 degrees

32) Once sample has reached 40 degrees, shut down poling

a. Set voltage to zero, click update voltage

b. Once voltage reaches zero, stop program with red stop sign at top left

c. Turn off power supply, multimeter, temperature controller, oxygen sensor, humidity sensor, and nitrogen regulator at tank.

Resource Management

When poling every day, plan on 10 nitrogen tanks per month

- This figure accounts for miscellaneous nitrogen use in clean room also
- Nitrogen contract with Airgas, call 1-800-666-6523, customer number SWF86

Flexible probe tip was made out of a copper part from inside a rotary switch. The switches come from bench stock. The copper part was then soldered to a wire cut off one side of a resistor, and this wire could then be put inside the standard probe mount.

Manuals for all meters and supplies involved are in Lab 10.

5 Teng & Man Experimentation

5.1 Introduction

5.1.1 Motivation

The motivation for this series of experiments was to use an interim poling setup and support an investigation of a technique to measure the electro-optic coefficient of different chromophores proposed by Teng and Man[2]. Samples poled were 15% CPW1, 21% CPW1, 21% CPW1 buffered on both sides by a UV15 layer, 8% FN2, and 40% FN2. This method is based on poling material samples by placing a probe in contact with an electrode rather than through corona poling.

5.1.2 Time Frame

This series of experiments took place between 20 Aug 02 and 29 Jan 03.

5.1.3 Personnel Involved

Brian Flusche, Franz Haas, Paul Cook, and Tom McEwen

5.2 Setup Description

We used the interim poling setup described in 3.1 for this test. A diagram of the samples we produced for this test is shown in Figure 5-1. We used glass slides with a thin indium tin oxide (ITO) coating on one side and masked a portion of the ITO face was masked with tape. These slides were then dipped in a solution of aqua-regia for five minutes to etch away the exposed ITO[3]. After etching, the tape was removed and the samples were baked out for at least an hour to remove excess solution. The ITO that had been masked in this process served as the ground electrode, while the etched areas provided an area to place the top electrode and not be concerned with shorting the sample. Next, the slides were again masked with tape, and a layer of core material was spun on. The tape was removed and the samples were sputtered with gold, resulting in a thin layer of gold on the sample that served as the top electrode. The probe carrying voltage from the supply, referred to later as the hot probe, was touched down on the top gold electrode of our sample, and the circuit was completed by touching a ground probe down to the ITO. The wire from the ground probe was connected back to the voltage source. In addition to the Oriel power supply, we also built a power supply that was capable of continuous or pulsed operation.

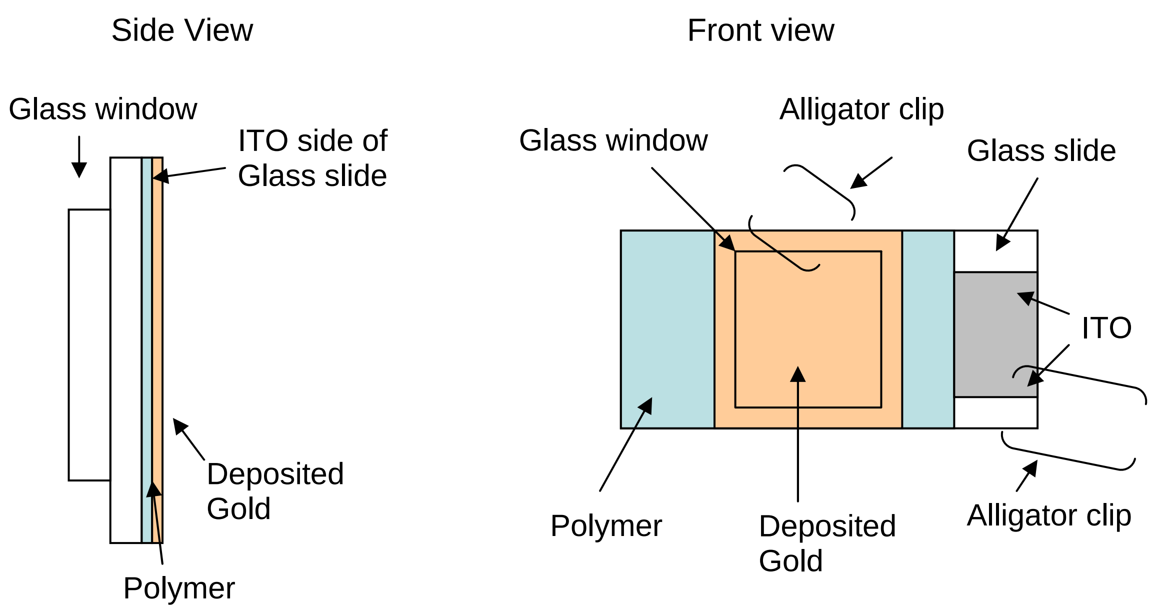

Figure 5-1. Teng & Man Sample Design

5.3 Experimental Objectives

The following issues were examined for this experiment. A brief, bottom-line answer follows each objective with full details in the Experimental Results section.

1) What poling temperature returns the optimum r33 for CPW1?

   => 150° C

2) Does reversing the direction of the applied electric field but holding the magnitude constant affect the r33?

   => No

3) Does buffering a chromophore sample on both sides with a thin layer of UV-15 affect the r33?

   => Yes, buffering the sample seems to increase r33

4) Does pulsed poling the chromophore with periodic surges of high voltage give a better r33 than simply poling with a constant high voltage?

   => No

5) Does extending the time at poling temperature from 15 minutes up to an hour affect r33?

   => Yes, extending the poling time seems to reduce the dependence of r33 on incident test angle

5.4 Procedure

Once we prepared samples of a given chromophore, we developed a poling protocol for each. The sample under test was placed inside our interim poling box. The box was then closed and sealed with blue tack tape.

Looking through a microscope, we first put the ground electrode in place on the ITO band using enough force to ensure the sample was locked in place. The hot electrode was placed second. The sample design and ITO etching process allowed us to place the probe without fearing that we would punch through the gold and short out the sample. Next, the nitrogen regulator was set to 10 psi in order to purge the poling chamber, and left on for 10 minutes. All room lights were then turned off. As the heating profile was begun, the regulator was lowered to 2 psi to conserve nitrogen. The temperature controller was then programmed with the desired heating profile. A typical profile is shown in Figure 5-2.

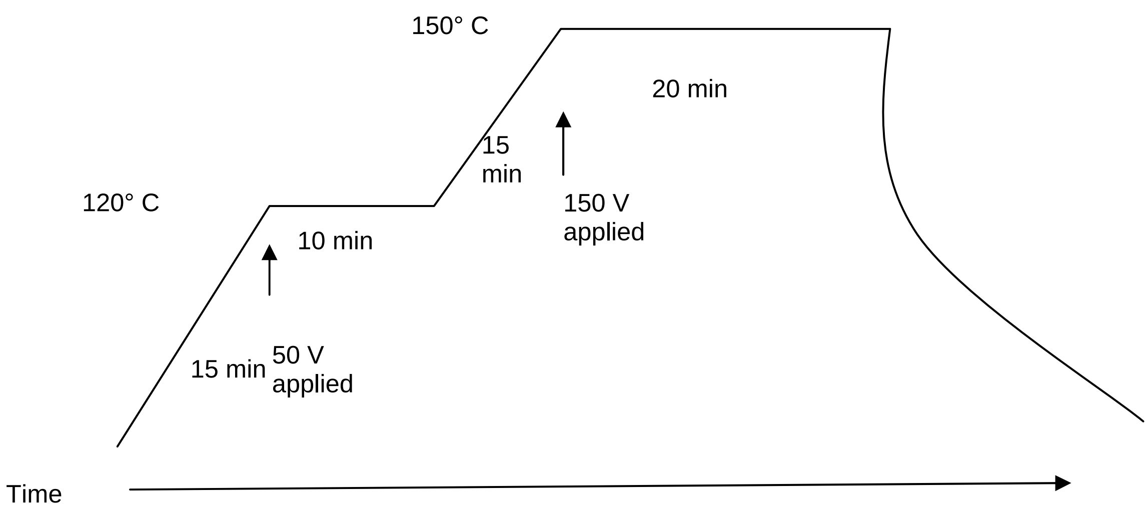

Figure 5-2. Typical Teng & Man Test Poling Profile

Although the parameters might vary, the general idea was to ramp first to a temperature plateau and stay there for some period of time, allowing the sample to boil off any water trapped in the polymer. When the plateau was reached, a small amount of voltage, typically 50V, was applied. The intent here was not to begin poling the device, but to determine if the sample was shorted due to the effects of material defects amplified by the temperature. In addition, it was hoped that a small electric field would keep molecules from aggregating as they gradually became free to move. Next, the heater would ramp to the desired poling temperature, and stay for as long as needed. When the poling temperature was reached, we slowly ramped up the voltage, with the intent being to maximize the applied voltage without destroying the sample. Our benchmark became stabilizing the applied voltage when we saw current activity in the sample, and we defined current activity as at least .3 uA measured on an ammeter placed on the ground side of the circuit created by the power supply, probes, and the sample. After this time, the controller shut off and the sample was left to passively cool with the nitrogen regulator almost completely closed, reducing flow to a trickle.

5.5 Experimental Results

Twenty three samples were poled and evaluated for this experiment. See Table 1 for a description of samples. 15% CPW1 was used only for a few samples to stabilize our sample prep technique. For 21% CPW1, we observed current activity in our samples at 150V, and decided to keep that constant and vary temperature. We determined 150° C was the optimum poling temperature for this chromophore. It appeared that reversing the direction of the applied electric field had no effect on r33. Buffering samples with UV-15 layers seemed to return a much higher r33 value. It is not known whether this is an artifact of the setup, assumptions in calculations, or an actual phenomenon. Pulsed poling resulted in a lower r33 than simply poling at a constant high voltage of 150V. Extending the poling time of the sample beyond 15 minutes up to an hour seemed to make r33 less dependent on incident angle of the test laser beam, but the peak value of r33 decreased.

5.6 Observations

This section is an attempt to document lessons learned about the poling process that can be carried forward to improve the next series of tests.

5.6.1 Light Sensitivity

These chromophores are light sensitive. Significant ambient room light results in a much higher current in the device under test, often causing it to catastrophically fail. Our setup still required the use of a small flashlight to read gauges and write notes, and it would be great to eliminate this altogether.

5.6.2 Oxygen Sensitivity

These chips are also sensitive to oxygen. If not poled in a nitrogen environment, the applied voltage is likely to destroy the device in question.

5.6.3 Current Limiting Resistor

We developed the idea of putting a large 10MΩ resistor in series with the device, thereby limiting the maximum amount of current able to drop across the device. This prevented the device from failing in more than one instance.

5.6.4 Probe Issues

The U shape of our probe was functional, but not the best solution. We often had issues with the probe punching through the gold electrode layer once the sample had reached the poling temperature. A delicate touch was needed when lowering the probe into position to ensure that there was enough force to keep the probe from bouncing on the sample during the process, but avoiding too much force which would result in the probe punching through to the core layer. The method finally settled on to correctly place the probe was lowering it while the sample was at room temperature until we observed the probe beginning to slide. Finally, perhaps the thin shape of the probe was susceptible to charge concentration, often causing destructive effects due to extreme voltages at the small point where the probe actually touched the electrode.

5.6.5 Interim Poling Setup

It is important to note that the setup used for these tests was originally intended as an interim setup to allow us to quickly make this capability available and allow us to identify important parameters requiring control in our final setup. This setup has been superceded by a stainless steel glove box setup and is no longer in use.

6 FN3 Experimentation

6.1 Introduction

6.1.1 Motivation

The motivation for this series of experiments was to support Fazio Nash in efforts to develop modulators with a new chromophore, called FN3.

6.1.1.1 Chromophore Description[4]

The goal of making devices with FN3 was to look at the effects of loading density vs. temperature. On FN3, cyclohexylthiophene unit was added to increased steric hindrance while providing adequate solubility in polycarbonate hosts. A high loading density of 35 weight percentage was chosen to test this concept. AM1 theoretical calculations predict a modest electro-optic coefficient of r33 ~ 20– 25 pm/V at 15 – 20% loading. In a 2 cm, single electrode Mach-Zhender device, this would correspond to a half-wave voltage of 7.1V.

FN3

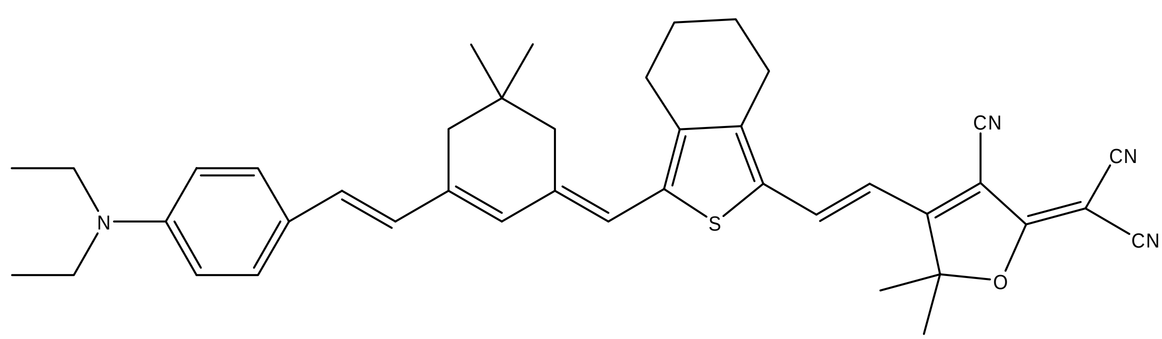

Figure 6-1. FN3 Chromophore Molecule

6.1.1.2 Wafer Fabrication Description

These samples were polymer modulator chips made on a silicon wafer having a lower metal ground plane, a lower cladding, a core material of 35% FN3 molecules by weight percentage in amorphous polycarbonate (APC), and an upper cladding material. See Figure 1-1. Polymer Modulator for a description of the material stack. We patterned gold electrodes on top of this material stack. Each wafer produced three low speed chips, with two Mach-Zhender modulators per chip. Figure 6-2 is a view of a typical wafer, showing the position of each individual chip. It is important to note that three of the chips had a 2 cm active electrode and two had a 1 cm active electrode.

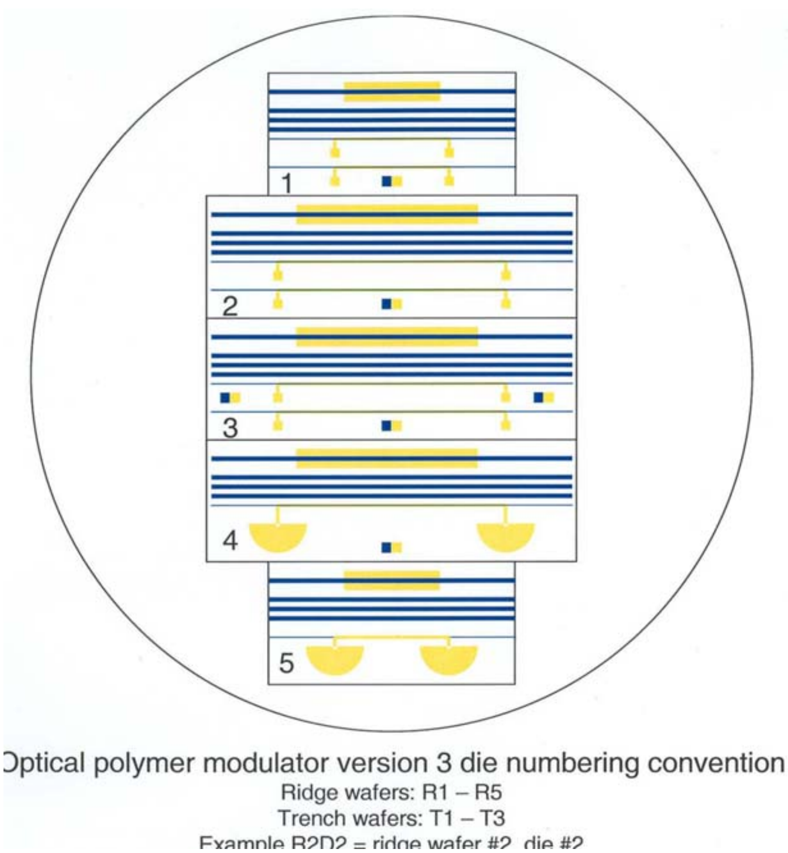

Figure 6-2. Device Layout On Typical Wafer

The 1 cm devices are expected to have a Vπ twice as large as the 2 cm devices. Therefore, in order to compare chips to each other, we based all our results on equivalent Vπ, which is defined as the actual Vπ of a 2 cm device or ½ the Vπ of a 1 cm device. This equivalent Vπ assumes an ideal correlation between the length of the electrode and Vπ.

6.1.2 Time Frame

These experiments took place between 9 May 03 and 7 Oct 03.

6.1.3 Personnel Involved

Brian Flusche, Franz Haas, and Fazio Nash

6.2 Setup Description

We used the stainless steel glove box described in 3.2 for this set of experiments. At the time this experiment was performed, we had not yet developed the probe tip described in 3.2. We started with an Alessi pointed probe tip that had been bent into a U shape. In addition, we had not yet received the Keithley multimeter and were using a digital Fluke meter to monitor the current running through the device. This meter gave resolution down to tenths of a microamp. In addition, we had not yet developed any LabVIEW programs to control and monitor the poling process.

6.3 Experimental Objectives

The following issues were examined for this experiment:

1) Would using the same poling profile from the Teng & Man experiments, but changing the poling temperature plateau to 115 C or 125 C and applied high voltage to 400V give us working devices?

   => Yes, but these devices had a poor $V\pi$

2) Would a new poling profile, consisting of applying 400V at the beginning of the test and ramping directly to poling temperature, give us working devices?

   => No

3) Would using the above new profile, but changing the amount of voltage applied from 400V to 750V, give us better devices?

   => No, and this demonstrated poling induced photo bleaching

6.4 Procedure

First, we scraped off an area of the chip clear to expose a ground electrode. The chip was then placed in an aluminum holder and inserted into the vacuum oven. The door was closed, and the vacuum line opened. The oven was vacuumed down to 50 kPa. At this point, the nitrogen purge valve was opened, with the regulator set to 10 psi. Nitrogen was allowed to flow until the vacuum gauge read 10 kPa, at which point the valve was closed and vacuuming began again. This process of purge-and-vacuum was repeated two more times. After the purge process is complete, we turned off the nitrogen flow to the oven at the cylinder. The chips would be left to bake out for at least three hours before poling. In order to prepare the poling chamber, the oxygen and humidity sensors were turned on about an hour before the chamber was needed. The oxygen sensor needed thirty minutes to warm up and begin reading, but the humidity sensor could begin reading and purging with nitrogen immediately, with the flow meter set above 20. The chamber was considered ready when the oxygen sensor read below 2.0 percent. At this point, we turned on the nitrogen cylinder connected to the vacuum oven, so that we could open the purge valve and bring the oven back to atmospheric pressure. We opened the inner oven door, pulled a chip out, and set it on the hot plate. Here we had to be sure to turn off the nitrogen cylinder attached to the oven, otherwise it would continue to run and drain the tank. The oven was resealed, returned to vacuum, and the camera, light source, and television were then turned on. The ground probe was placed first because we could press on it significantly without having to worry about punching through the material and shorting the sample. In this manner, the ground probe also serves to fix the chip in place. We placed the hot probe next, paying careful attention to the pressure applied to ensure we didn't punch through. Next, the black curtain was lowered to shield the poling box from light, and the TV and camera were shut off. The nitrogen flow meter was set to 17 in order to keep the poling chamber at low oxygen levels but not waste nitrogen. All room lights were then turned off. We used two different poling protocols which are described below.

6.4.1 FN3 Poling Protocol #1

The first was a new poling protocol devised by Fazio Nash and is shown in Figure 6-3. The poling voltage (up to 750V) was applied when heating started, and voltage was left constant for the entire run. With voltage already applied, the temperature controller programmed to ramp directly from room temperature to the poling temperature (typically 125° C) over a 45 minute period. The controller would then hold 125° C for 30 minutes. It is important to note that this new profile was the same length of time as our profiles developed for our Teng & Man testing. After this time, the controller shut off and the sample was left to passively cool, with the nitrogen regulator settings unchanged.

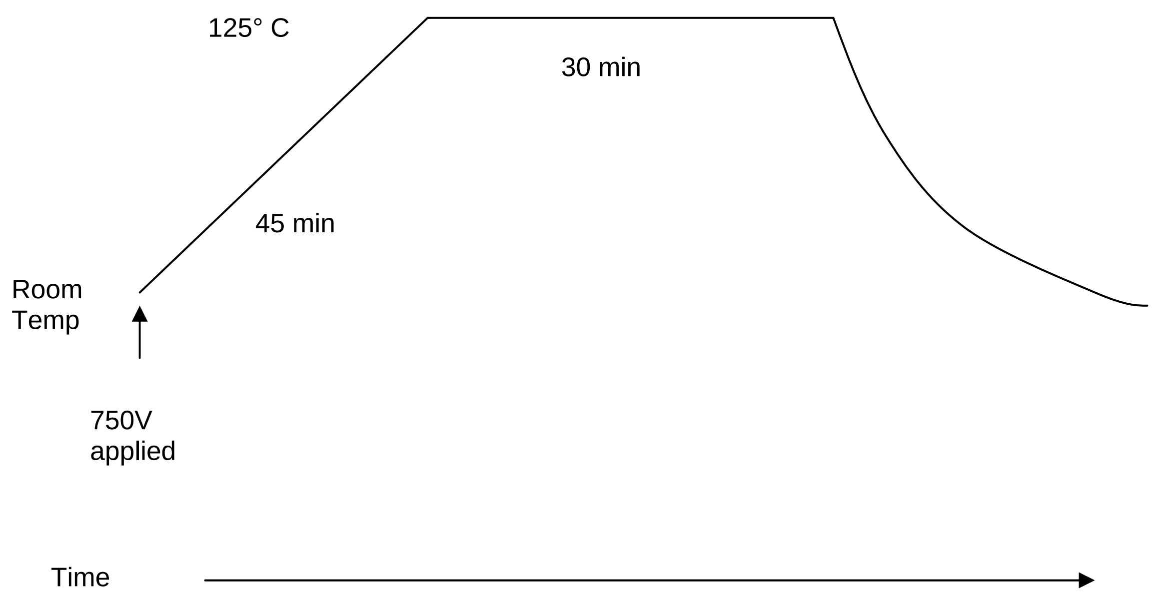

Figure 6-3. FN3 Poling Profile #1

6.4.2 FN3 Poling Protocol #2

The second poling protocol used was a variation of our Teng & Man CPW-1 profile and is shown in Figure 6-4. The temperature controller was programmed to ramp from room temperature to 100° C over a 15 minute period. When the plateau was reached, 50V was applied. The intent here was not to begin poling the device. Rather, it was a simple check to determine if the sample was shorted due to the effects of material defects amplified by the temperature. In addition, it was hoped that a small electric field would keep molecules from aggregating as they gradually became free to move. In addition, this temperature plateau allowed the sample to outgas. Next, the heater would ramp to the desired poling temperature over 15 minutes. When the poling temperature was reached, we slowly ramped up the voltage until we reached 500V. The controller would then maintain the desired poling temperature for the desired poling time, which was typically 20 minutes. After this time, the controller shut off and the sample was left to passively cool, with the nitrogen regulator untouched.

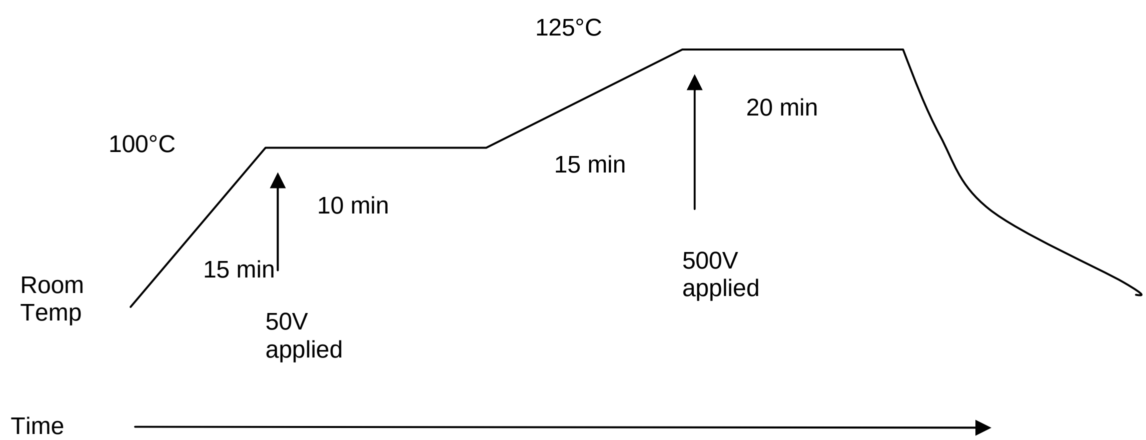

Figure 6-4. FN3 Poling Profile #2

6.5 *Experimental Results*

Twenty four samples were poled and tested for this effort. See Table 1 for a list of poled devices.

6.5.1 Results for FN3 Poling Protocol #1

Using both 400V and 750V, no working devices were produced using this new protocol.

6.5.2 Results for FN3 Poling Protocol #2

Working devices were produced with this protocol, which was essentially a modification of the CPW-1 profile developed during our Teng & Man testing. The optimum parameters of this protocol, a poling temperature of 115° C and 400V applied, produced devices with a Vπ around 20V. Poling at 125° C but keeping voltage constant at 400V seemed to increase Vπ slightly. Poling at 115° C but reducing voltage to 300V seemed to increase Vπ. Poling at 115° C but increasing voltage to 500V resulted in devices that would not modulate.

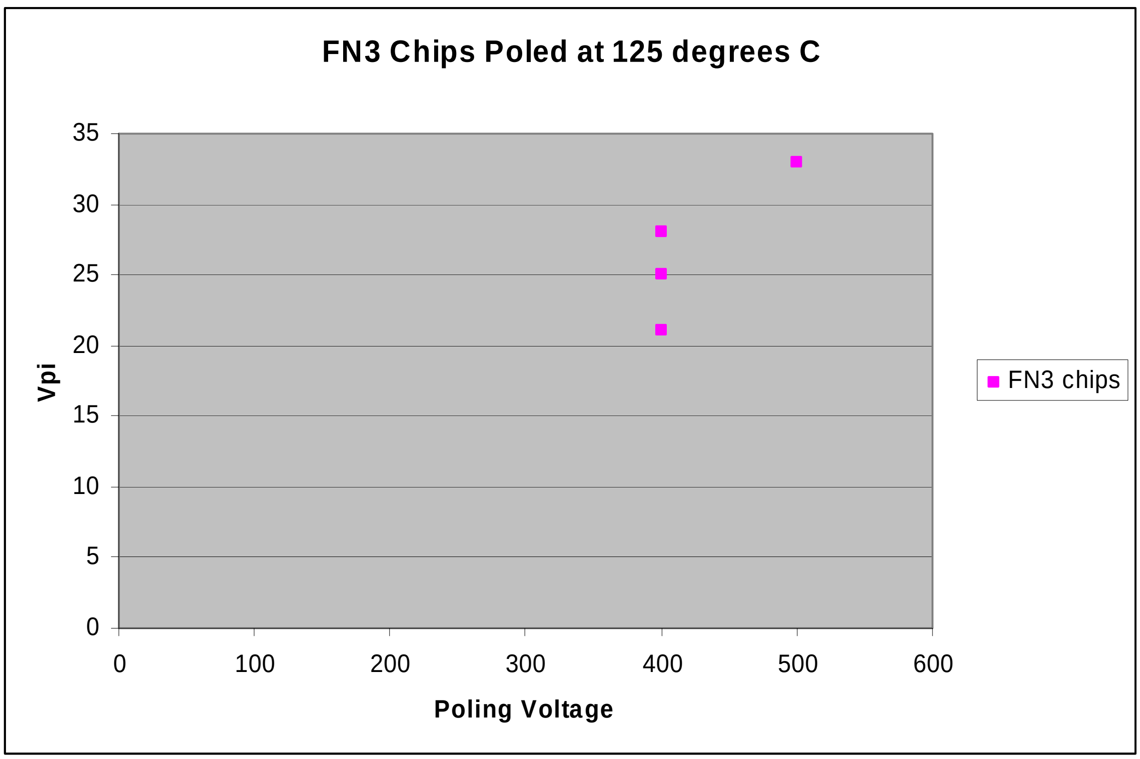

Figure 6-5. FN3 Voltage vs. Vπ Successfully Poled With Protocol #2 at 125° C

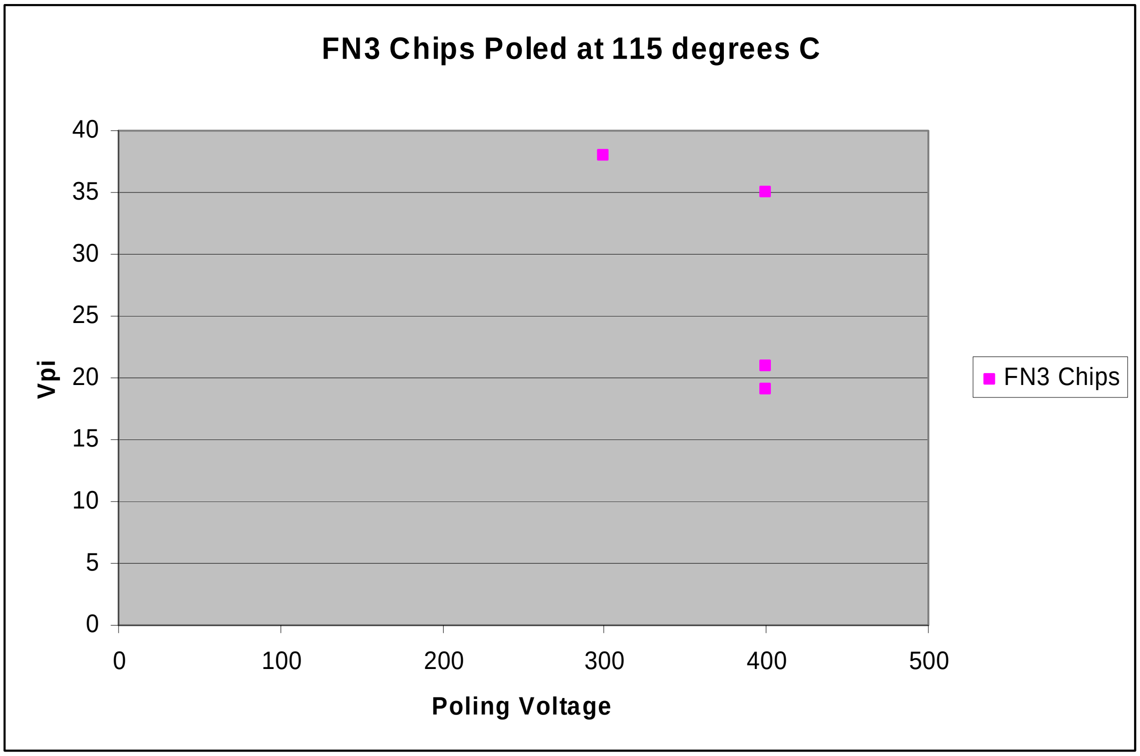

Figure 6-6. FN3 Voltage vs. Vπ Successfully Poled With Protocol #2 at 115° C

6.5.3 Disparity Between Theory and Results

The team was in general disappointed with these results, but the consensus within the team was that the films were loaded too heavily with chromophore molecules. This was reflected in that the films were very optically lossy, and seemed to get more lossy as Vπ decreased. This meant that the closer we got to optimizing Vπ, the farther we got from a useful product. However, much had been learned for the next iteration of FN chromophores.

6.6 Observations

This section is an attempt to document lessons learned about the poling process that can be carried forward to improve the next series of tests.

6.6.1 Voltage drop across the core

There was some debate among the team whether contact poling of a device could drop enough voltage across the core or whether most of the voltage was dropped across the cladding materials. During poling with the new protocol, where 750V was applied at start of program, one sample seemed to demonstrate we had applied too much voltage, resulting in bleaching the chromophore, shown in Figure 6-7. A portion of the electrode micro strip was blown apart and curled back on itself, showing that the core material had changed from dark blue to yellow underneath the poling electrode. When tested, the devices poled under this protocol did not guide light, which we assume was because the refractive index of the core material was changed enough such that the optical waveguides could no longer guide light. The lesson we took from this was that voltage was being dropped across the core material, rather than across the cladding as some on the team had feared. In addition, we confirmed that the application of too much voltage causes poling induced photo bleaching.

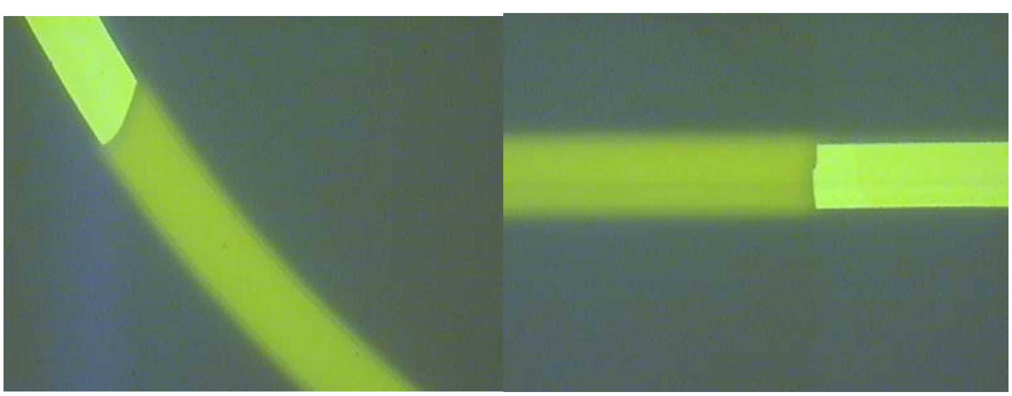

Figure 6-7. Poling Induced Photo Bleaching of FN3

7 CPW-1 Experimentation

7.1 *Introduction*

7.1.1 Motivation

The motivation for this series of experiments was to fabricate devices as described in 6.1.1 with a core material made of CPW-1, a chromophore with known characteristics, in order to ensure we had optimized our fabrication process. A second goal was to produce many devices poled under consistent conditions to be used as samples for radiation testing of our polymer modulators. These devices were made with a core material of 25% CPW-1 by weight percentage in APC.

7.1.2 Time Frame

These experiments took place between 9 May 03 and 17 Nov 03.

7.1.3 Personnel Involved

Brian Flusche, Franz Haas, Fazio Nash, Attila Szep, and Jared Caffey

7.2 *Setup Description*

We used the stainless steel glove box setup described in 3.2. It was during this experiment that we developed the final probe tip described in 3.2. We started with just an Alessi pointed probe tip that had been bent into a U shape. We went through several iterations of new probe tips to ensure contact with the electrode but minimize the risk of punching through the material and shorting the device. The first attempted change was placing a small folded piece of aluminum foil underneath the Alessi probe tip in order to better distribute the probe's pressure and offer a wider profile for contacting the electrode. The second change was to replace the Alessi probe tip and aluminum foil with a completely new tip. We made a tip out of wire cut off of a resistor and soldered to a relatively flat, relatively flexible copper piece from a rotary switch. We named this our “shovel probe”, since the profile it created upon touching down on the sample resembled the wide curved back of a shovel, as opposed to the trench dug by the old Alessi probe tip.

7.3 Experimental Objectives

The following issues were examined for this experiment:

1) Would using the optimum temperature poling profile from the Teng & Man experiments, but changing the poling voltage applied to 450V give us working devices with a consistently low Vπ and little chromophore bleaching?

    => Yes

2) In order to increase poling throughput, is it possible to produce working devices by covering a wafer of CPW-1 devices with gold and poling the entire wafer at one time, then etching the top layer of gold off leaving only the micro strip electrodes above the wave guides?

    => Yes, but this technique still has many challenges to overcome

3) Is there a better probe tip than the U-shaped Alessi tip?

    => Yes, the copper “shovel” probe is far superior

7.4 *Procedure*

7.4.1 Chip scale poling

We used the same procedure described in 6.4 to prepare the chips for poling and position them in the poling chamber. We used a single poling protocol derived from our Teng & Man test results, shown in Figure 7-1, for all the chip scale poling activities to ensure consistency. The temperature controller was programmed to ramp from room temperature to 120° C over a 15 minute period. At this point, 50 volts were applied to ensure the electrodes of the sample were not shorted out. The controller would then hold 120° C for 10 minutes. Next, the controller would ramp to 150° C over 15 minutes. After reaching 150° C, the controller would hold that temperature for 20 minutes. This gave us time to slowly increase the voltage to 450V and still allow at least 15 minutes of poling time at temperature with full voltage applied. After this time, the controller shut off and the sample was left to passively cool, with the nitrogen regulator untouched.

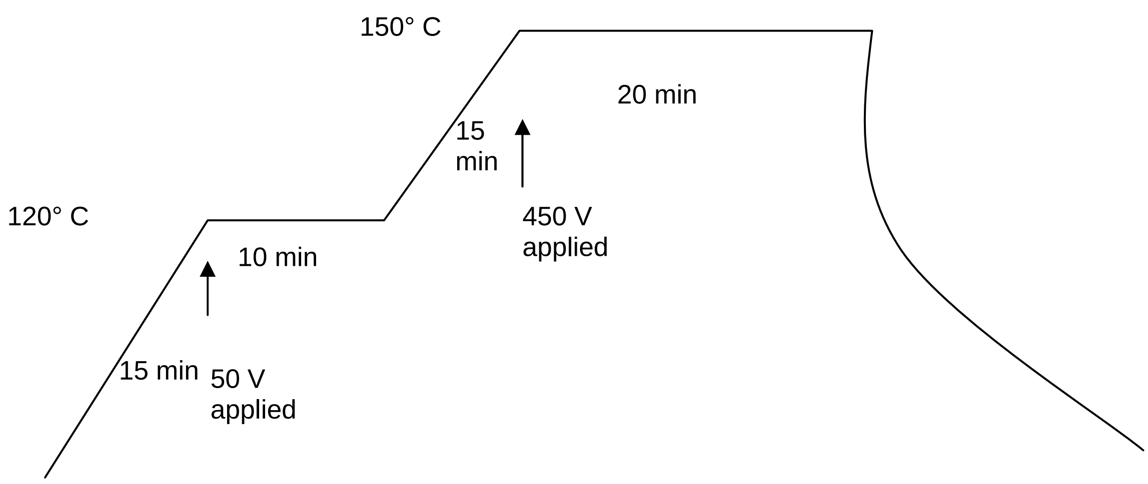

Figure 7-1. July 2003 25% CPW-1 Chip Scale Poling Profile

7.4.2 Wafer scale poling

The procedure for wafer scale poling was the same as chip scale poling, with the three exceptions discussed below. After poling, the wafers were etched to remove the gold layer, leaving the drive electrodes, and diced into individual chips.

7.4.2.1 Voltage differences

We initially intended to take the wafer scale samples to 450V to keep consistency with the chip scale samples. However, it quickly became apparent that our power supply could not support this, as it would often display a “V trip” error message stating that a voltage trip had occurred, and turn off the voltage. It is important to note that we were dealing with a much larger capacitor as we compare the gold covered wafer to a single gold covered device. Our solution was to experiment on the first few wafers to find a suitable voltage not susceptible to the V trip. We experimented and were able to successfully reach 300V, 350V, and 400V, but never 450V. 400V became the standard for the bake out experiments that would occur later.

7.4.2.2 Probe positioning differences

Since we were poling the entire wafer at one time, we had a large contact area and didn’t have to worry about hitting a particular electrode. We electroplated up two very large, thick gold pads on each wafer, and these pads were very easy to simply drop the hot probe on without having to worry about punching through the gold. Additionally, they were thick enough to support the extensive current flowing through them, which often peaked at 500 mA.

7.4.2.3 Bake out differences

Since wafer scale poling samples were mostly covered in gold, we were concerned about excess amounts of solvent being trapped in the core. To address this, we ran a small experiment on some wafers after identifying the optimum voltage. We kept all parameters among them the same, but baked the wafers out in the vacuum oven at 115° C from one to five days before poling. 115° C was chosen because it was above the solvent's boiling point.

7.5 Experimental Results

7.5.1 Chip scale poling

Twenty seven samples were poled and tested for this effort. See

Table 2 for a list of poled devices. $V\pi$ ranged from 5V to 7V for our better devices. Several devices poled were of a more dubious quality, with $V\pi$ around 10V to 12V. On these devices, we suspect the probe was bouncing in and out of contact with the sample due to the polymer expanding and shrinking as the temperature changed. The third group was chips with a $V\pi$ of more than 16V. These chips were ones where the probe popped loose early on in the poling run, removing the field while chromophores were still easily able to move around. However, this shows that our poling protocol can produce good devices. It is important to note that the outlier chips with Vπ greater than 50 were both from the same wafer. This suggests that there was an alignment error when the devices were fabricated, such that the electrodes were not totally over the wave guides.

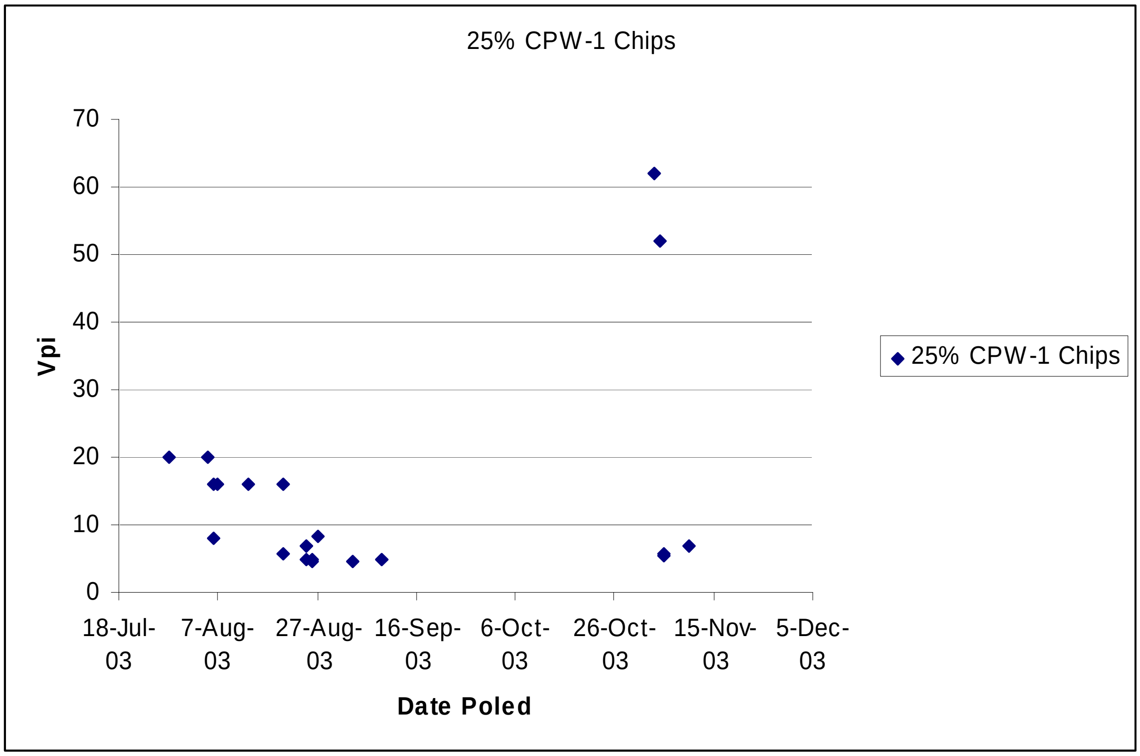

Figure 7-2. July 2003 25% CPW-1 Devices Poled With the Same Profile

7.5.2 Wafer scale poling

Eight wafers were poled and evaluated for this effort. After etching the gold away from the wafers, we confirmed that trapped solvents had a significant destructive effect on the wafers during poling. The polymer was delaminated around the bubbles and the chromophore had actually changed colors in these regions. Our bake-out experiment was successful in reducing bubbles, with a five day bake-out at 115° C resulting in a wafer with less than five bubbles. Only a few working devices were produced, but the chips off of one of these wafers had a $V\pi$ of 4.4V. Although wafer poling has many challenges, it can produce effective devices and is worth investigating further.

7.5.3 Probe issues

Using aluminum foil underneath the probe did not ensure any better contact. It was very difficult to get the aluminum foil exactly flat and in contact with the gold. Since we couldn't rely on the foil to provide us with a level swath of electrical contact, it was actually harder to hit the electrode because the foil obscured the camera's view. On the other hand, the copper shovel probe worked very well. The tip was compliant enough to handle the pressure needed to fix it in place and ensure it didn't bounce. In addition, the wide footprint of the probe ensured contact was maintained through the expansion and contracting of the polymer without punching through.

7.6 Observations

This section is an attempt to document lessons learned about the poling process that can be carried forward to improve the next series of tests.

7.6.1 Wafer poling bubbles

After the first wafer poling run, we discovered that the wafer was covered with hundreds of bubbles underneath the gold, where the metal had apparently delaminated from the polymer. In order to determine what was causing this, we cleaved the edges off of another wafer, giving us a few samples to test with voltage and temperature. For the first test we took a sample and ran it through the heating profile of a standard poling run, but applied no voltage. This test resulted in no bubbles. Next, we took another shard and ran it through the voltage profile of a standard poling run, applying voltages at the normal times and levels but with the chip remaining at room temperature. Again, no bubbles were observed. Last, we took a shard of the wafer through a complete poling profile, applying voltage and temperature as if it were an actual device. After the combination of voltage and heat, the shard was covered in bubbles. We suspect that some solvent is trapped in the core during fabrication. As poling proceeds, this solvent is released when the combination of temperature and voltage allows the chromophore molecules to begin aligning.

7.6.2 Bake-out results

A potential solution to the observed bubbling effect is to try to drive off the trapped solvent by baking the wafers out. We baked a series of wafers out from one to five days at 115° C and then ran the procedures described in 6.4.2 on each. After poling, it was clear that increasing the bake-out time directly correlated to producing less bubbles. We stopped the experiment at five days of bake-out because this produced a wafer with less than five bubbles. It was off of this wafer with minimal bubbling that the 4.4V V_π chips were obtained.

8 Deuterated Methanol on CPW-1 Experimentation

8.1 Introduction

8.1.1 Motivation

The motivation for this series of experiments was to fabricate devices with CPW-1 similar to those described in 7.1.1 but use deuterated methanol in the fabrication process instead of regular methanol. We thought the deuterated methanol might reduce optical loss in our devices. A second goal was to produce many devices to be used as samples for radiation testing and long term temperature testing of our polymer modulators. These chips were made of 29% CPW-1 by weight percentage in APC.

8.1.2 Time Frame

These experiments took place between 11 Dec 03 and 29 Mar 04.

8.1.3 Personnel Involved

Brian Flusche, Fazio Nash, Jared Caffey, Brian McKeon, and Attila Szep

8.2 Setup Description

We used the stainless steel glove box setup described in 3.2. Additionally, we developed a LabVIEW program that could automate the poling process by managing the temperature controller, multimeter, and power supply. The program designed the poling profile according to the user's inputs and tracked temperature, voltage, and current data, saving them for later review.

8.3 Experimental Objectives

The following issues were examined for this experiment:

1) Would using the optimum temperature poling profile from the previous 25% CPW-1 devices also be the most effective for the deuterated methanol 29% CPW-1 devices?

   => No, protocol #4 described in 8.4.4 yielded better devices

2) Could we develop a poling protocol to allow a deuterated methanol 29% CPW-1 device to perform at least as well as our 25% CPW-1 chips from the July fabrication run?

   => Yes, the 29% CPW-1 devices performed better than the 25% CPW-1 devices

3) Once the optimum poling temperature has been identified, could increasing the poling voltage above 450V produce better results?

   => Yes, experimentation documented in Figure 8-6 demonstrated 550V was the optimum voltage

8.4 Procedure

We used the same procedure described in 6.4 to prepare the chips for poling and position them in the poling chamber. Four main poling protocols were used, and they are described in detail below. Some additional experimentation was done to further investigate temperature and voltage effects.

8.4.1 Protocol #1

Our intent was to use the poling protocol from 7.4.1, replacing the poling temperature of 150° C with our guess of 160° C. The reason for changing our poling temperature was the thought that a higher concentration of chromophore would require an increase in temperature.

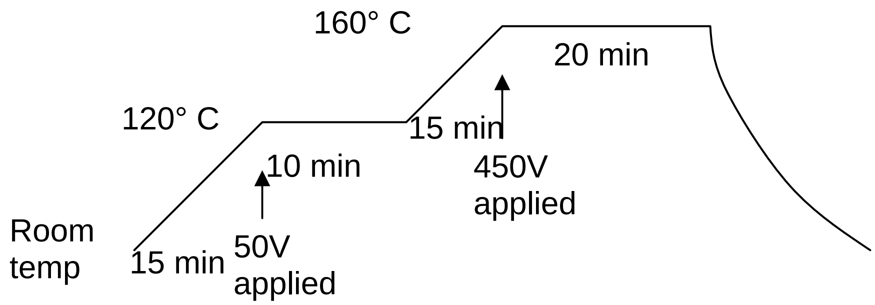

Figure 8-1. 29% CPW-1 Poling Protocol #1

8.4.2 Protocol #2

On one run, while following poling protocol #1 described in 8.4.1, we realized the probe was not properly set in contact with the electrode as we were applying the poling voltage of 450V. To remedy this, we replaced the probe and then re-applied 450V. We then extended the poling time by eight minutes so that the chip would be at 160° C for the same length of time as our other chips. However, this meant that the chip had been sitting at 160° for eight minutes with no voltage applied, and spent a total of 28 minutes at 160°. In addition, this meant that there was no voltage at all on the chip until 48 minutes into the poling process.

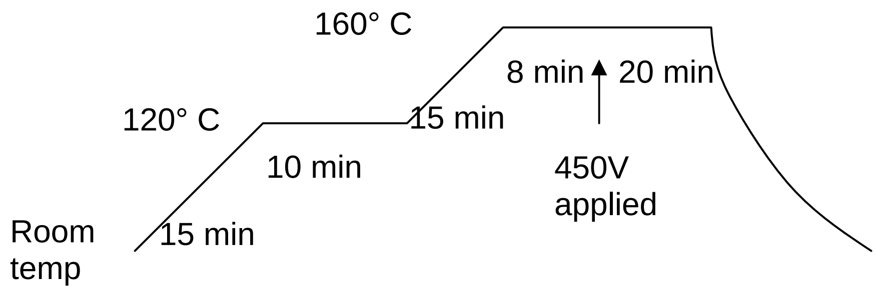

Figure 8-2. 29%CPW-1 Poling Protocol #2

8.4.3 Protocol #3

Another thought was to pole some chips using the exact poling protocol from 7.4.1, just to see how they compared to chips from our July 2003 fabrication run.

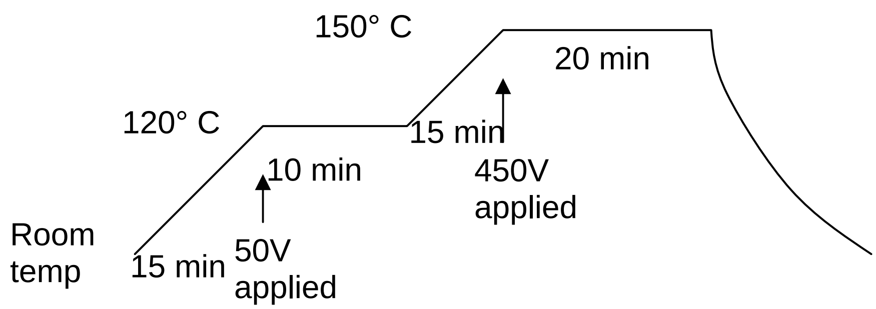

Figure 8-3. 29% CPW-1 Poling Protocol #3

8.4.4 Protocol #4

A fourth step was to replicate protocol #2 from 8.4.2, but poling at 150° C instead of 160° C.

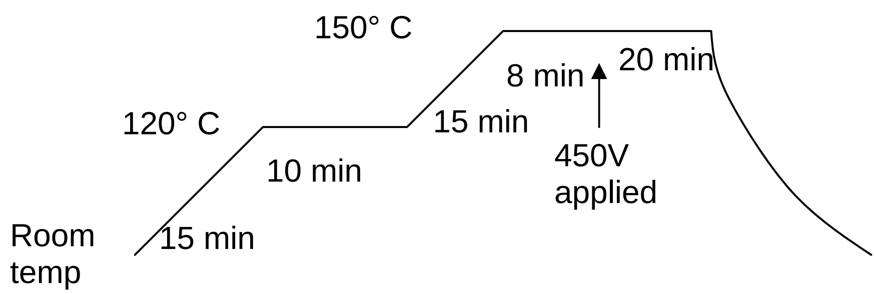

Figure 8-4. 29% CPW-1 Poling Protocol #4

8.4.5 Additional temperature experiments

We next used protocol #4 described in 8.4.4 but varied the poling temperature, replacing 150° C with the temperature we wanted to test.

8.4.6 Additional voltage experiments

In order to determine the optimum poling voltage, we used protocol #4 described in 8.4.4 but varied the applied voltage in 50V increments between 450V and 650V.

8.5 Experimental Results

See Table 3 for a detailed list of poled and tested devices. Figure 8-5 shows how V_π can vary as the poling temperature profile is changed and poling voltage is held constant.

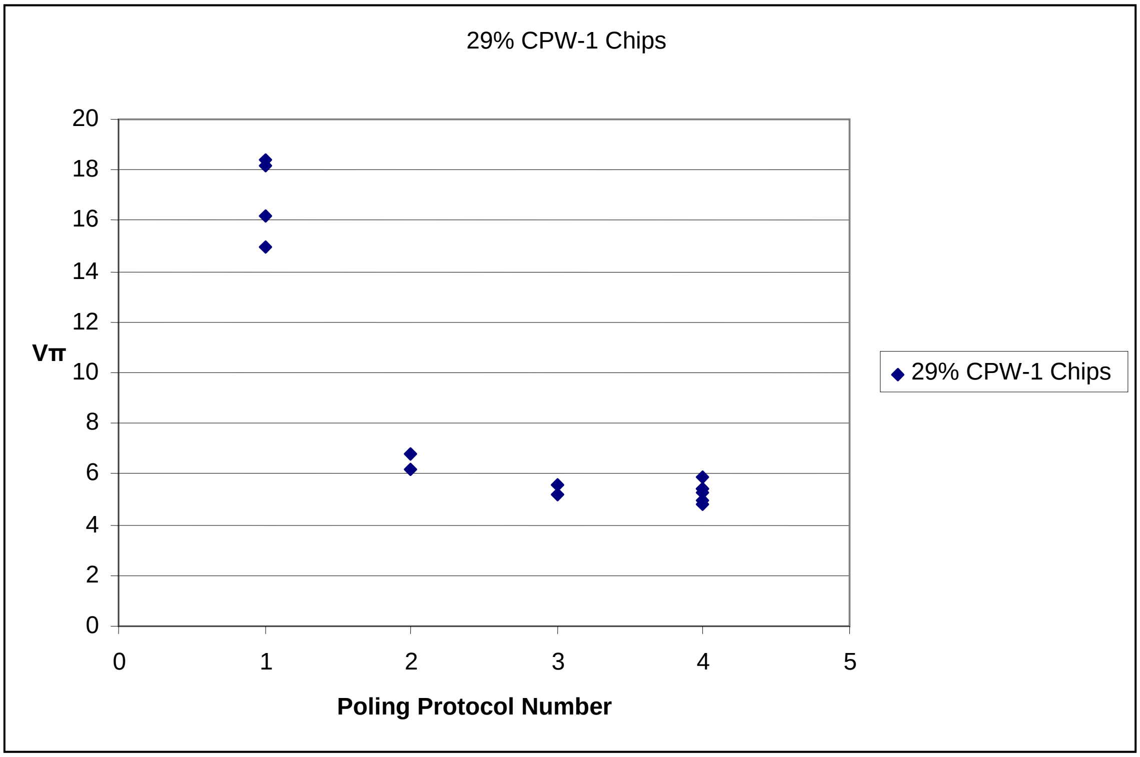

Figure 8-5. December 2003 29% CPW-1 Chips Poled at 450V With Different Temperature Profiles

8.5.1 Initial temperature experimentation

Four chips were poled according to the protocol described in 8.4.1, with Vπ results being between 15V and 18V. Two chips were poled according to protocol #3 described in 8.4.3, with both chips having a Vπ of 5.2V. This gave us the information we needed to settle on 150° C versus 160° C.

8.5.2 Timing experimentation

Two chips were poled according to protocol #2 described in 8.4.2, with Vπ results being between 6V and 7V. Two chips were poled according to the protocol described in 8.4.4, both producing a Vπ of 4.8V.

8.5.3 Additional temperature experimentation

Using the protocol described in 8.4.5, we tested 138° C, 140° C, 146° C, and 148° C. These tests suggest that 150° C was the ideal temperature and that performance degraded as the temperature was changed.

8.5.4 Voltage experimentation

Using the protocol described in 8.4.6, we discovered that Vπ did decrease as voltage was increased until hitting 550V, where a Vπ of 4.2V was achieved. Above 550V, Vπ actually began to increase again as voltage increased.

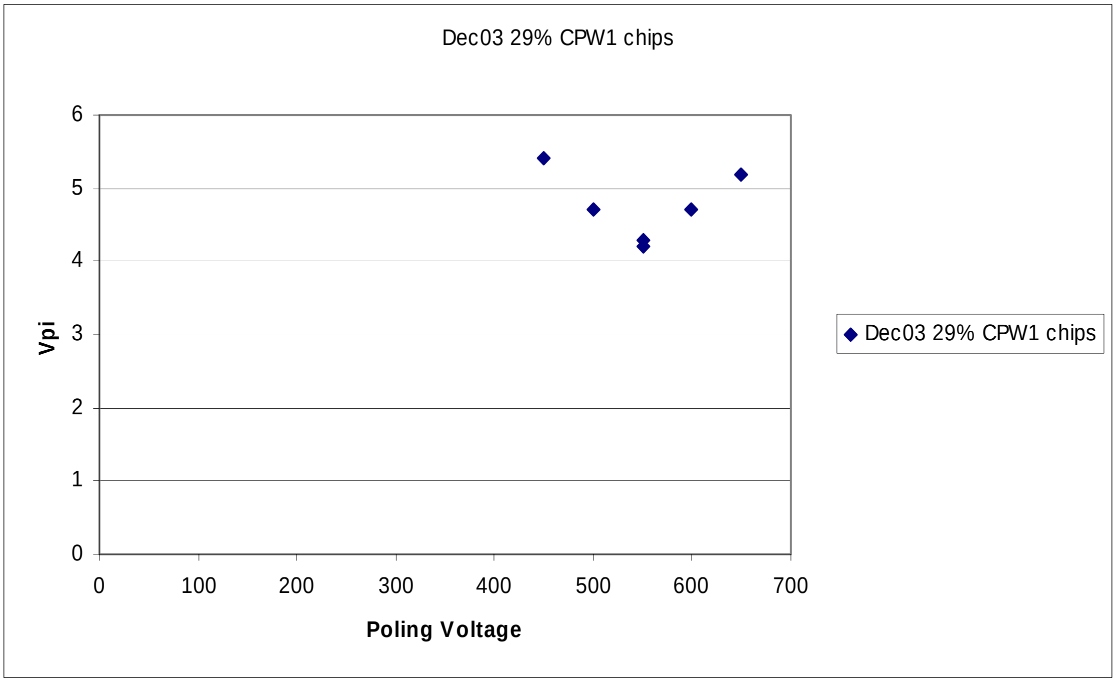

Figure 8-6. Poling Voltage vs. Vπ

8.6 Observations

This section is an attempt to document lessons learned about the poling process that can be carried forward to improve the next series of tests.

8.6.1 Timing of the probe drop

Conventional wisdom among our team at the beginning of these experiments held that if the chromophore was heated to the glass transition temperature without an electric field applied, the dipole charges would cause the molecules to bind to each other. This would result in fewer dipoles available to contribute toward $V\pi$, which should result in a higher $V\pi$. Our experiments documented in 8.5.2 demonstrated that for CPW-1 at least, this was not the case. Therefore, this eight minute delay before dropping the probe has been incorporated into our standard poling methods. Further investigation as to the optimum wait time before dropping the probe could prove very valuable.

8.6.2 Increasing voltage

Our team also often debated what the optimum voltage was. Our experiments documented in 8.5.4 demonstrated that while higher voltage improved the r33 of the core material, at some point, this improvement was outweighed by the percentage of chromophore molecules being destroyed and therefore $V\pi$ would increase. This effect is shown in Figure 8-6, and it clearly demonstrates a decrease in performance before the material breakdown point is attained.

8.6.3 LabVIEW current observations

The sensitivity of our Keithley multimeter combined with the LabVIEW program allowed us to very accurately monitor the current in the device being poled. This produced several positive results.

8.6.3.1 Probe contact

After poling enough devices, we began to identify trends in the shape of the current profile as it was graphed onscreen in the LabVIEW program. Figure 8-7 represents an “ideal” poling run, giving the good, consistent, repeatable result we were looking for.

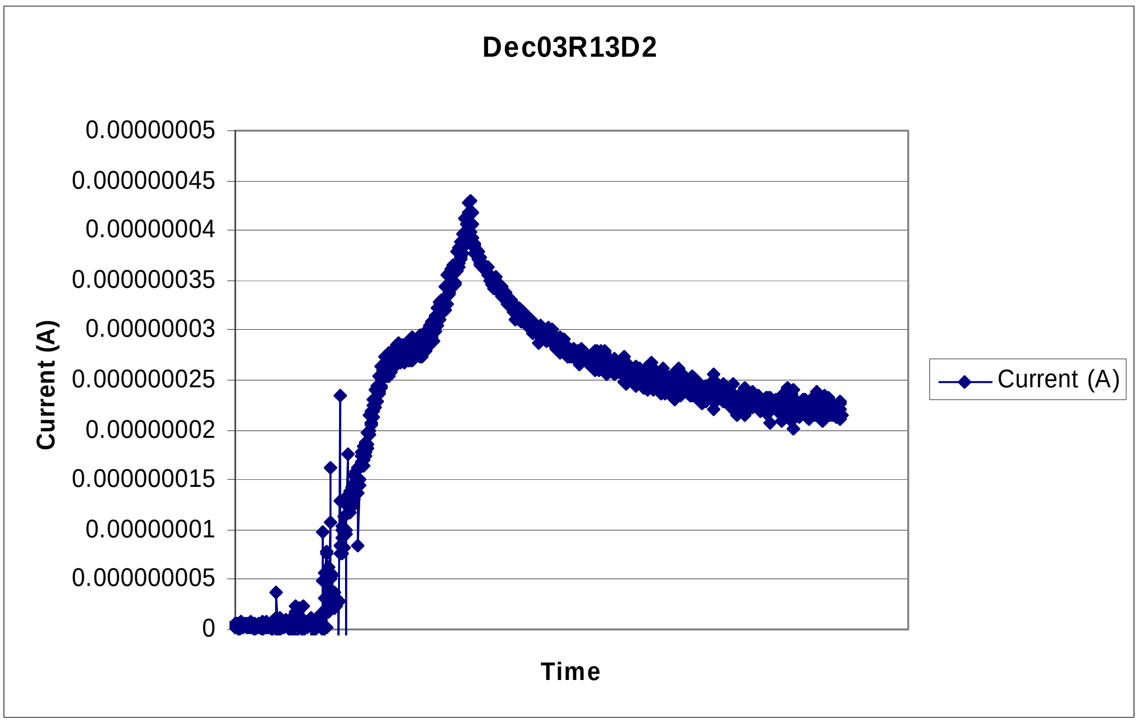

Figure 8-7. Ideal Current Profile in 29% CPW-1 Device

Figure 8-8, on the other hand, represents a scenario where the probe was not applied with enough pressure and began to bounce as the chip flexed due to rising temperature.

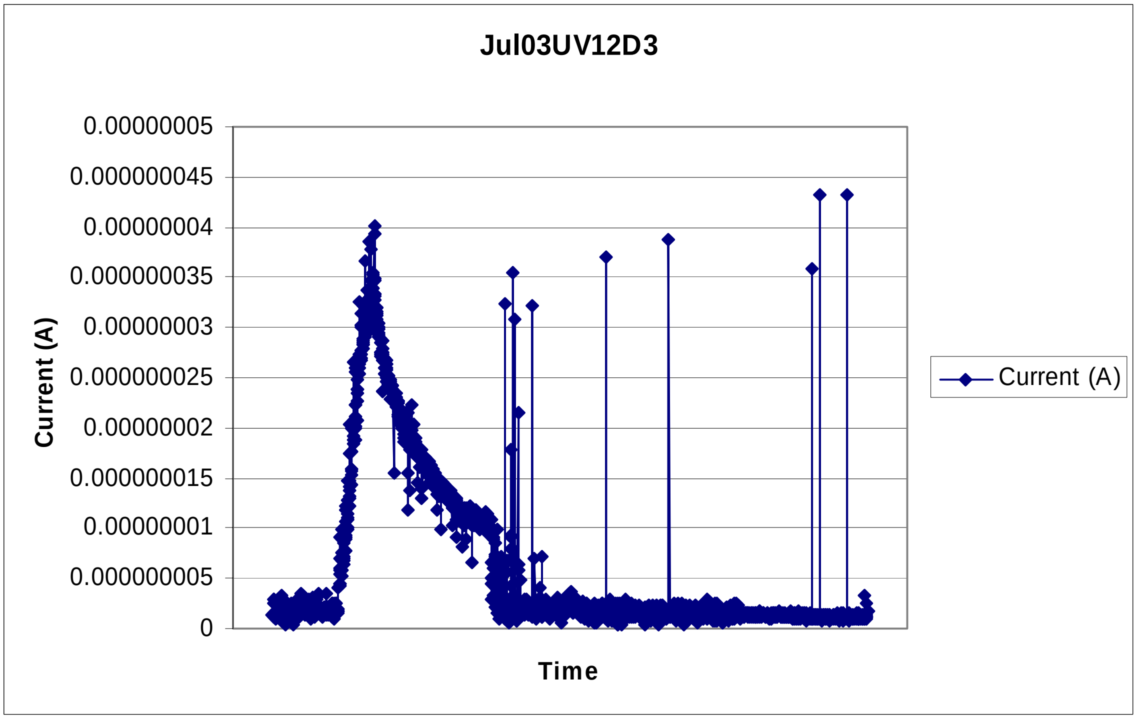

Figure 8-8. Current Profile of 25% CPW-1 Demonstrating Bouncing Probe

Through these graphs, the user could identify a problem within seconds and quickly take the required action to ensure the device poled correctly. Without this data, the user would only be aware of a problem when a sub-standard Vπ was reported by the testing team. At that point, the team is unsure whether a probe issue, fabrication problem, or a poling parameter caused the poor Vπ. We encountered this scenario during poling of the July fabrication run, but since all parameters were the same, we knew it was probe issues. The LabVIEW tracking program eliminates this problem.

8.6.3.2 Voltage versus current profile

During the experimentation described in 8.5.4 we observed how the graphical shape of the current profile changed as the voltage increased. See Figure 8-9 to see how the current profile changed. It is important to note that two of the current profiles are labeled as “equivalent current”. This is because they were 1 cm devices and had to be scaled to compare with 2 cm devices. Since total current is a function of current density multiplied by the area of the electrode, a good scaling factor is to multiply the observed current in a 1 cm device by two for comparison with 2 cm devices.

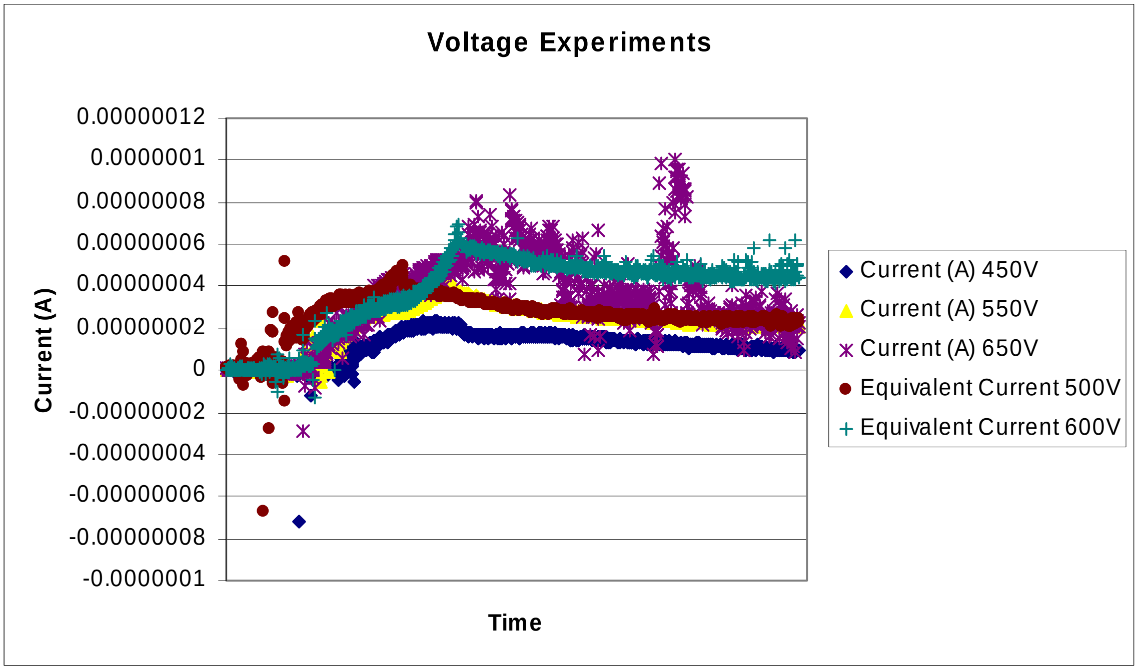

Figure 8-9. Current Profile Varying According to Poling Voltage in CPW-1 Devices

An interesting point for further investigation is whether the shape of the current profile produced during the poling of our best chip is consistent from chromophore to chromophore. Put another way, knowing what the ideal current profile is for 29% CPW-1, can we predict the optimum poling voltage of other chromophores solely through the poling process?

8.6.4 Optical loss

The goal of using deuterated methanol in the fabrication process was to determine if it reduced optical loss in the chips. Test results of chips made in December 2003 showed their loss to be very similar to chips made in July 2003, and yet the December chips yielded better $V\pi$. As chromophore loading density is increased, we expect optical loss to the increase. The fact that a higher chromophore loading density reduced $V\pi$ while loss stayed constant indicates that the deuterated methanol had a positive impact. The data suggests that further investigation would be worthwhile and needed to definitively prove this.

9 Future Experimentation and Raw Data

9.1 Data Points

It is important to note that some of the issues presented here are conjectures due to the limited number of samples. More samples should allow the team to fully investigate these areas if further attention is required as the project proceeds.

9.2 Poling Protocol Experimentation

The standard method of determining an optimum poling protocol for a brand new chromophore will probably require about 30 devices. This number accounts for devices needed for temperature experimentation, voltage experimentation, and attrition due to damaged devices.

9.2.1 Temperature Experimentation

A reasonable poling voltage, like 400V, should be chosen in order to strike a balance between enhancing $V\pi$ while avoiding chromophore bleaching. At this point, a best guess for the Tg should be determined, along with potential upper and lower bounds. Pole at the best guess Tg and halfway to the bounds on either side. Observe any trends, and pole again halfway between data points in the direction desired. It is worth noting that a five degree difference in poling temperature can have a significant impact on $V\pi$.

9.2.2 Voltage Experimentation

Upon deciding on an optimum temperature, vary the poling voltage by 100V from the initial poling guess. Observe trends, and determine whether another 100V increase or decrease is required. If not, 50V resolution is required. Pole in between data points, and if desired, repeat at 25V increments to optimize voltage.

9.2.3 Timing Issues

It would be interesting to further investigate the reason that delaying the probe drop and high voltage application seem to improve $V\pi$ since we accidentally discovered this technique. Logical questions that follow from this are:

1) When is the optimum time to drop the probe and apply high voltage?
2) How does increasing or decreasing the poling time affect $V\pi$?
3) Does varying the pre-poling bake out time of chips affect $V\pi$?

9.3 Final Questions

There are a few lingering questions that should be investigated:

1) How does changing chromophore loading density affect optimum poling voltage and Tg?
2) Is the Tg of the core material in a particular host a material property of the guest chromophore material, strictly the chromophore loading density, or a mix of both? What factors can lead us to accurately predict Tg?

9.4 Raw Data

Table 1. FN3 Chip Data

Chip Name	Vπ (V)	Straight Total Loss (dB)	Extinction Ratio (dB)
FN3 - Standard Electrode			
Jul03F1D1	25	47	
Jul03F1D2	16+	36	
Jul03F1D3	21	34	
Jul03F3D1	No mod		
Jul03F3D2	No mod		
Jul03F4D1	30+	49	
Jul03F4D2	19	31	
Jul03F4D3	21		
Jul03F5D1	No mod		
Jul03F5D2	38		
Jul03F5D3	No mod		
Jul03F9D1			
Jul03F9D2	No guide		
Jul03F9D3	No mod		
R7D1	No mod		
R7D2	No mod		
R7D3	No guide		
R8D2	No guide		
R8D3	No guide		
R11D1	No guide		
R11D2	No guide		
R12D1	Damaged		
R12D2	33		8
R12D3	Damaged		
FN3 - Williams Electrode			
Jul03F9D4	No guide		
Jul03F9D5	No guide		
R8D5			
R11D4	No guide		
R11D5	16+		

Table 2. July 2003 25% CPW-1 Chip Data

Chip Name	Vπ (V)	Straight Total Loss (dB)	Extinction Ratio (dB)
CPW - Standard Electrode			
Jul03R4D1	6		
	32+	6.5	
Jul03R4D2	20		
	35.5	16.1	4.5
Jul03R4D3	20		
Jul03R6D1	Damaged	during poling	
Jul03R6D2	8.1		
	8.6	7.6	12.4
	9.2	7.6	12.8
Gamma Irradiated	9.2	7.8	10
Jul03R6D3	16+		
Jul03R7D1	11.2		10
	12	7.5	12.3
	11.6	7.1	10.2
Gamma Irradiated	12	7.1	14.7
Jul03R7D2	No mod		
Jul03R7D3	16+	16	
Jul03R8D1	16+	9.6	
Jul03R8D2	7		8

	7.2	8.3	11.1
	7	7.9	10.6
	6.8	16.4	5.9
	7.1	15.6	10.8
Proton Irradiated	7.4	8.1	9.3
Jul03R8D3	5	13	12
	5.2	8.3	10.7
	5.4	8.2	10.8
	5.4	16.1	10.4
	5.7	16.3	10
Proton Irradiated	5.7	8.9	10.5
Jul03UV7D1	9.3		16
	9.4	7.6	16.1
	9.6	7.6	13.5
	9.9	18.6	11.9
	9.9	18.6	12.4
	9.9	21.1	17
Proton Irradiated	10.2	8	14.5
Jul03UV7D2	8.2	17	14
	8.7	9.3	15.2
	9.2	9.6	8.5
Gamma Irradiated	9	10.3	17.1
Jul03UV7D3	4.9	9.6	12
	4.9	9.3	12.3
	5.2	9.6	10.6
Gamma Irradiated	5.2	Damaged	12.8
Jul03UV9D1	9.6		8
	9.8	8.2	14.6
	9.6	7.9	10.2
Gamma Irradiated	10.2	7.8	17.9
Jul03UV9D2	No mod		
Jul03UV9D3	4.9	11.4	7

	4.7	7.8	11.1
	4.9	7.9	13.3
Gamma Irradiated	5	8.1	7.2
Jul03UV12D1	No mod	6.9	
Jul03UV12D2	62		12.3
Jul03UV12D3	52	9	
Jul03UV13D1	11.2	8.2	11.7
	11.4	6.9	13.4
	11.1	17.7	15.8
Proton Irradiated	11.4	7.4	15.5
Jul03UV13D2	5.6	10.4	13.9
	5.8	10.3	10.6
Gamma Irradiated	5.8	10.8	11.4
Jul03UV13D3	7	8.5	15.2
Jul03T1D1	11.8	16	10
Jul03T1D2	13.6		9
Jul03T1D3	No mod		
April 2003 CPW - Irradiated Chips	Pre/Post		
R1D2	4.4 / 4.4		
R3D1	41 / --		
R3D2	44 / 48		
R3D3	7.7 / 6.9		
R5D2	29.3 / 27		
R17D1	27.6 / 28		
CPW - Williams Electrode			
Jul03R1D5			

Jul03UV7D4	5		
Jul03UV9D4			
Jul03R8D4			
CPW - Wafer poled, most damaged badly			
Jul03R3			
Jul03UV2			
Jul03UV4			
Jul03UV5			
Jul03UV6			
Jul03UV8			
Jul03UV10			
Jul03UV11			

Table 3. December 2003 29% CPW-1 Chip Data

Chip Name	Date Poled	Date Measured	Vπ (V)	Straight Loss (dB)	Extinction Ratio (dB)
CPW - Standard Electrode					
Dec03R4D1	15-Dec-03	10 Feb 04	12.4	7.6	11.35
Gamma Irradiated		9-Mar-04	12	8.6	15.7
Dec03R4D2	16-Dec-03		15		
Dec03R5D1	16-Dec-03		32.4	7.7	
Dec03R5D2	18-Dec-03		18.4	8.8	7.2
Dec03R5D3	18-Dec-03		18.2	9.5	
Dec03R6D1	19-Dec-03		13.6	8.5	
Dec03R6D2	19-Dec-		5.2		11.6

	03				
Gamma Irradiated		Damaged end facets, no coupling possible			
Dec03R6D3	5-Jan-04	12-Feb-04	5.6	10	10.5
Gamma Irradiated		9-Mar-04	5.2	9.9	16.3
Dec03R7D1	6-Jan-04	10-Feb-04	10.6	14.3	7
Gamma Irradiated		9-Mar-04	9.2	7.6	18.9
Dec03R7D2	7-Jan-04	10-Feb-04	5	8.7	11.5
Dec03R7D3	21-Jan-04	24-Mar-04	4.8		15.1
Dec03R9D1	22-Jan-04	24-Mar-04	11.8		25.2
Dec03R9D2	27-Jan-04	11-Feb-04	5.4	10.2	19.8
Gamma Irradiated		9-Mar-04	5.2	10.3	13.5
Dec03R9D3	28-Jan-04	11-Feb-04	5.4	9.4	20
Gamma Irradiated		Damaged during unpacking			
Dec03R10D1	10-Feb-04	Poling Tg experiment for Fazio			
Dec03R10D2	12-Feb-04	2-Feb-04	8.4	8.2	13
Gamma Irradiated		Damaged during unpacking			
Dec03R10D3	12-Feb-04	11-Mar-04	45+		
Dec03R11D1	25-Feb-04	11-Mar-04	24+		20+

Dec03R11D2	26-Feb-04	11-Mar-04	15.2		20+
Dec03R11D3	1-Mar-04	11-Mar-04	9.4		Poor
Dec03R12D1	1-Mar-04	Input facet scratched			
Dec03R12D2	13-Mar-04	15-Mar-04	6		13.6
Dec03R13D1	15-Mar-04	15-Mar-04	9.4		11.8
Dec03R13D2	15-Mar-04	16-Mar-04	4.6		11.3
		24-Mar-04	4.2		13.65
Dec03R13D3	25-Mar-04	25-Mar-04	5.2		15.05
Dec03R14D1	25-Mar-04	26-Mar-04	9.4		17.6
Dec03R14D2	29-Mar-04	29-Mar-04	4.2		12.1

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[4] Information provided by Dr. Fazio Nash, AFRL/SNDP, **2004**